REMARKS/ARGUMENTS

In the Office Action mailed July 22, 2008, claims 1 and 3-7 were rejected. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. For reference, claim 1 and claim 7 are amended to address antecedent basis issues. No claims are added or canceled.

Claim Rejections under 35 U.S.C. 112

Claims 1-7 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, claims 1 was rejected because it recites the limitation "sampling clock signals," and claim 7 was rejected because it recites the limitation "sampling clock signals."

Claim 1 and claim 7 are amended to address the antecedent basis issues. Accordingly, Applicants respectfully request that the rejections of claims 1 and 7 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 103

Claims 1 and 3-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pohlmeyer et al. (U.S. Pat. Pub. No. 2002/0101884, hereinafter Pohlmeyer) in view of Sato et al. (U.S. Pat. No. 5,596,582, hereinafter Sato). However, Applicants respectfully submit that these claims are patentable over Pohlmeyer and Sato for the reasons provided below.

Independent Claim 1

Applicants assert that claim 1 is patentable over Pohlmeyer and Sato for at least two reasons. First, Sato does not teach a sync break interval that matches the unique pattern for the specified bit period. Second, Pohlmeyer and Sato do not teach the supply of the sampling clock signal is suppressed after and end of a preceding message until said condition is met.

1. Sato does not teach a sync break interval that matches the unique pattern for the specified bit period.

Claim 1 recites "the clock source circuit verifying for each potential sync break interval whether the sync field interval identified by that potential sync break interval specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period, as a condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval identified by the potential sync break interval" (emphasis added).

In contrast, Sato does not teach a sync break interval that precedes the sync field interval. Sato does teach a synchronizing symbol within the data stream. Sato, Fig. 10, col. 9, lines 10-32. However, Sato does not teach a sync break interval that precedes the synchronizing symbol. Sato teaches that the sync frame is identified by moving a window bit by bit until a sync period is identified. Sato, col. 9, lines 33-62. Sato does not teach supplying the sampling clock signal based on the bit period determined by the sync break interval.

For the reasons presented above, the combination of Pohlmeyer and Sato does not teach all of the limitations of claim 1 because Sato does not teach a sync break interval that specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period, as a condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval identified by the potential sync break interval. Accordingly, Applicants respectfully assert claim 1 is patentable over Pohlmeyer and Sato because the combination of Pohlmeyer and Sato does not teach all of the limitations of claim 1.

2. Pohlmeyer and Sato do not teach the supply of the sampling clock signal is suppressed after an end of a preceding message until said condition is met.

Claim 1 recites "wherein the supply of the sampling clock signal is suppressed after an end of a preceding message until said condition is met" (emphasis added).

The Office Action states that the combination of Pohlmeyer and Sato fails to explicitly teach a supply of sampling clock signals is suppressed after an end of a preceding message until said condition is met. The Office Action asserts that Sato

purportedly suggests that a supply of sampling clock signals is suppressed after an end of a preceding message until said condition is met based on the teaching of "the supply of sampling clock signals depend on the detection of the synchronization patterns." Office Action, 7/22/08, p. 7 (citing text that is apparently not in Sato). However, Sato does not suggest suppressing the supply of the sampling clock signal until a condition is met.

Sato merely teaches that the frequency controller 61 is connected to the interval selector 57 and a controllable oscillator 63 is controlled by the frequency controller 61. Therefore, Sato teaches varying the frequency of the frequency controller based upon stored pattern sequences. Sato, col. 8, lines 32-49. However, Sato does not teach the supply of the sampling clock signal is suppressed after an end of a preceding message until said condition is met.

For the reasons presented above, the combination of Pohlmeyer and Sato does not teach or suggest all of the limitations of claim 1 because Sato does not suggest a supply of sampling clock signals is suppressed after an end of a preceding message until said condition is met. Accordingly, Applicants respectfully assert claim 1 is patentable over Pohlmeyer and Sato because the combination of Pohlmeyer and Sato does not teach all of the limitations of claim 1.

Independent Claim 7

Applicants respectfully assert independent claim 7 is patentable over the combination of Pohlmeyer and Sato at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 7 recites "supplying the sampling clock signal at a frequency adapted to the timing property of the sync field interval on the condition that the sync break interval matches the unique pattern for the specified bit period, wherein the supply of the sampling clock signal is suppressed after an end of a preceding message until said condition is met" (emphasis added).

Here, although the language of claim 7 differs from the language of claim 1, and the scope of claim 7 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 7. Accordingly, Applicants respectfully assert claim 7

is patentable over the combination of Pohlmeyer and Sato because the combination of Pohlmeyer and Sato does not teach all of the limitations of the claim.

Dependent Claims

Claims 3-6 depend from and incorporate all of the limitations of the corresponding independent claim 1. Applicants respectfully assert claims 3-6 are allowable based on an allowable base claim. Additionally, each of claims 3-6 may be allowable for further reasons, as described below.

In regard to claim 4, Applicants respectfully submit that claim 4 is patentable over the combination of Pohlmeyer and Sato because the combination of cited references does not teach all of the limitations of the claim. Claim 4 recites "wherein the clock source circuit is arranged furthermore to verify whether one or more internal intervals between communication signal level changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval as a further condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval" (emphasis added). The Office Action cites Sato (Figs. 7 and 10, interval detector 59; col. 9, lines 51-62), and purports that Sato suggests the limitation because "the interval detector measures a time interval F between two maxima" and "synchronization patterns are used to make the frequency converter control the controllable oscillator." While Sato does teach using synchronization patterns to make the frequency converter control the controllable oscillator, as stated above, Sato does not teach the limitation of claim 4 because Sato does not teach changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval as a further condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval. Sato does not use a sync field interval to supply the sampling clock signal because Sato does not teach a data stream with a sync field interval. While Sato does teach a method to control the controllable oscillator, Sato does not teach changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval as a further condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval.

Accordingly, Applicants respectfully assert that claim 4 is patentable over Pohlmeyer and Sato because Sato does not teach the indicated limitations.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the proposed amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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Date: October 17, 2008

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